What Is Claimed Is:

1. A method for forming a shallow trench isolation structure in a semiconductor device comprising:

forming a trench in a substrate;

forming an oxide layer on sidewalls and a bottom of the trench;

forming a metal or poly-silicon layer on the oxide layer;

etching a portion of the metal or poly-silicon layer to expose the oxide layer on the bottom of the trench while leaving the metal or poly-silicon layer on the sidewalls of the trench; and

depositing a dielectric material layer to fill the trench.

2. A method as defined in claim 1, wherein the trench is formed in the substrate by an RIE (Reactive Ion Etching) method.

3. A method as defined in claim 1, wherein the oxide layer contains LP-TEOS oxide or thermal oxide.

4. A method as defined in claim 1, wherein the metal or poly-silicon layer contains poly-silicon, a laminated metal of Ti, TiN and W, or a laminated metal of Ta, TaN and W.

5. A method as defined in claim 1, wherein the dielectric material layer contains oxide.

6. A method as defined in claim 1, wherein the dielectric material layer is deposited by using an HDP CVD (High Density Plasma Chemical Vapor Deposition) method or an O_3-TEOS CVD (Ozone - Tetra Ethyl Ortho Silicate Chemical Vapor Deposition) method.

7. A method as defined in claim 1, wherein forming the trench in the substrate comprises:

forming a LP-TEOS (Low Pressure Tetra Ethyl Ortho Silicate) oxide layer on a surface of the substrate;

forming a nitride layer on the LP-TEOS oxide layer;

forming a PR pattern on the nitride layer;

forming a LP-TEOS oxide pattern and a nitride pattern by etching the LP-TEOS oxide layer and the nitride layer using the PR pattern as a mask;

removing the PR pattern; and

etching the substrate to a predetermined depth using the nitride pattern as a mask.

8. A method as defined in claim 7, wherein forming the LP-TEOS oxide layer on the surface of the substrate and forming the nitride layer on the LP-TEOS oxide layer are performed by using a LPCVD (Low Pressure Chemical Vapor Deposition) method.

9. A method as defined in claim 7, wherein forming the LP-TEOS oxide pattern and the nitride pattern by etching the LP-TEOS oxide layer and

the nitride layer is performed by an RIE method.

10. A method for forming a shallow trench isolation structure comprising:

(a) forming a trench in a substrate;

(b) forming a first oxide layer on sidewalls and a bottom of the trench;

(c) forming a second oxide layer on the first oxide layer;

(d) forming a PSG (Phosphor Silicon Glass) layer on the second oxide layer; and

(e) depositing a USG (Undoped Silicon Glass) layer to fill the trench.

11. A method as defined in claim 10, wherein the trench is formed in the substrate by an RIE method.

12. A method as defined in claim 10, wherein the first oxide layer contains LP-TEOS oxide or thermal oxide.

13. A method as defined in claim 10, wherein the second oxide layer contains HDP CVD oxide or O_3-TEOS oxide.

14. A method as defined in claim 10, wherein the PSG layer is deposited by an HDP CVD or O_3-TEOS CVD method.

15. A method as defined in claim 10, wherein the USG layer is deposited by an HDP CVD or O_3-TEOS CVD method.

16. A method as defined in claim 10, wherein forming the trench in the substrate comprises:

forming a LP-TEOS (Low Pressure Tetra Ethyl Ortho Silicate) oxide layer on a surface of the substrate;

forming a nitride layer on the LP-TEOS oxide layer;

forming a PR pattern on the nitride layer;

forming a LP-TEOS oxide pattern and a nitride pattern by etching the LP-TEOS oxide layer and the nitride layer using the PR pattern as a mask;

removing the PR pattern; and

etching the substrate to a predetermined depth using the nitride pattern as a mask.

17. A method as defined in claim 16, wherein forming the LP-TEOS oxide layer on the surface of the substrate and forming the nitride layer on the LP-TEOS oxide layer are performed by an LPCVD method.

18. A method as defined in claim 16, wherein forming the LP-TEOS oxide pattern and the nitride pattern by etching the LP-TEOS oxide layer and the nitride layer is performed by an RIE method.